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PTO/SB/21 (04-04)

TRANSMITTAL FORM (to be used for all correspondence after initial filing)	Application Number	10/798,597
	Filing Date	March 10, 2004
	First Named Inventor	Xiaobao Wang
	Art Unit	Unassigned
	Examiner Name	Unassigned
Total Number of Pages in This Submission	Attorney Docket Number	015114-054911US

ENCLOSURES (Check all that apply)		
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SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT		
Firm or Individual name	Townsend and Townsend and Crew LLP Steven Cahill Reg. No. 44,578	
Signature		
Date	8/30/04	

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PATENT
Attorney Docket No.: 015114-054911US
Client Reference No.: A1250

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

Xiaobao Wang et al.

Application No.: 10/798,597

Filed: March 10, 2004

For: TECHNIQUES FOR PROVIDING
MULTIPLE TERMINATION
IMPEDANCE VALUES TO PINS ON
AN INTEGRATED CIRCUIT

Examiner: Unassigned

Art Unit: Unassigned

INFORMATION DISCLOSURE
STATEMENT UNDER 37 CFR §1.97 and
§1.98

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

The references cited on attached form PTO/SB/08A and PTO/SB/08B are being called to the attention of the Examiner. Copies of the non-patent references are enclosed. It is respectfully requested that the cited references be expressly considered during the prosecution of this application, and the references be made of record therein and appear among the "references cited" on any patent to issue therefrom.

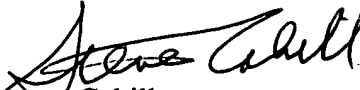
As provided for by 37 CFR §1.97(g) and (h), no inference should be made that the information and references cited are prior art merely because they are in this statement and no representation is being made that a search has been conducted or that this statement encompasses all the possible relevant information.

Applicant believes that no fee is required for submission of this statement.

However, if a fee is required, the Commissioner is authorized to deduct such fee from the

undersigned's Deposit Account No. 20-1430. Please deduct any additional fees from, or credit any overpayment to, the above-noted Deposit Account.

Respectfully submitted,


Steven Cahill
Reg. No. 44,578

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60294322 v1



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**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**

(use as many sheets as necessary)

Sheet 1 of 3

Complete if Known

Application Number	10/798,597
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Examiner Name	Unassigned
Attorney Docket Number	015114-054911US

U.S. PATENT DOCUMENTS*

Examiner Initials*	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number Kind Code ² (if known)			
	1	US-6,489,837	12-03-2002	Schultz et al.	
	2	US-6,466,063 B2	10-15-2002	Chen	
	3	US-6,448,813 B2	09-10-2002	Garlepp et al.	
	4	US-6,445,245 B1	09-03-2002	Schultz et al.	
	5	US-6,424,169 B1	07-23-2002	Partow et al.	
	6	US-6,411,126 B1	06-25-2002	Tinsley et al.	
	7	US-6,366,128 B1	04-02-2002	Ghia et al.	
	8	US-6,362,644 B1	03-26-2002	Jeffery et al.	
	9	US-6,356,106 B1	03-12-2002	Greeff et al.	
	10	US-6,329,836 B1	12-11-2001	Drost et al.	
	11	US-6,252,419 B1	06-26-2001	Sung et al.	
	12	US-6,236,231 B1	05-22-2001	Nguyen et al.	
	13	US-6,181,157 B1	01-30-2001	Fiedler	
	14	US-6,157,206	12-05-2000	Taylor et al.	
	15	US-6,154,060	11-28-2000	Morriss	
	16	US-6,147,520	11-14-2000	Kothandaraman et al.	
	17	US-6,118,310	09-12-2000	Esch, Jr.	
	18	US-6,100,713	08-08-2000	Kalb et al.	
	19	US-6,097,208	08-01-2000	Okajima et al.	
	20	US-6,087,847	07-11-2000	Mooney et al.	
	21	US-6,064,224	05-16-2000	Esch, Jr. et al.	
	22	US-6,049,255	04-11-2000	Hagberg et al.	
	23	US-6,037,798	03-14-2000	Hedberg	
	24	US-6,026,456	02-15-2000	Ilkbahar	
	25	US-6,008,665	12-28-1999	Kalb et al.	
	26	US-5,970,255	10-19-1999	Tran et al.	
	27	US-5,955,911	09-21-1999	Drost et al.	
	28	US-5,939,896	08-17-1999	Hedberg	
	29	US-5,864,715	01-26-1999	Zani et al.	
	30	US-5,764,080	06-09-1998	Huang et al.	
	31	US-5,726,583	03-10-1998	Kaplinsky	
	32	US-5,726,582	03-10-1998	Hedberg	
	33	US-5,721,548	02-24-1998	Choe et al.	
	34	US-5,623,216	04-22-1997	Penza et al.	
	35	US-5,602,494	02-11-1997	Sundstrom	
	36	US-5,592,510	01-07-1997	Van Brunt et al.	
	37	US-5,374,861	12-20-1994	Kubista	
	38	US-5,359,235	10-25-1994	Coyle et al.	
	39	US-5,179,300	01-12-1993	Rolandi et al.	
	40	US-5,164,663	11-17-1992	Alcorn	
	41	US-5,134,311	07-28-1992	Biber et al.	

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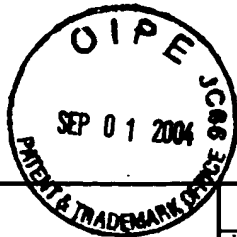
Substitute for form 1449A/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use as many sheets as necessary)			Complete if Known		
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U.S. PATENT DOCUMENTS+					
Examiner Initials*	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number Kind Code ² (if known)			
	42	US-5,111,081	05-05-1992	Atallah	
	43	US-4,954,729	09-04-1990	Urai	
	44	US-4,719,369	01-29-1988	Asano et al.	

FOREIGN PATENT DOCUMENTS								
Examiner Initials*	Cite No. ¹	Foreign Patent Document			Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T ⁶
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60294322 v1



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STATEMENT BY APPLICANT**

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Sheet 3 of 3

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First Named Inventor	Xiaobao Wang
Art Unit	Unassigned
Examiner Name	Unassigned
Attorney Docket Number	015114-054911US

NON PATENT LITERATURE DOCUMENTS

Examiner Initials *	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
	45	"Apex 20K Programmable Logic Device Family," product data sheet, version 3.7, May 2001 Altera Corporation San Jose, CA (2001).	
	46	"Apex II Programmable Logic Device Family," product data sheet, version 1.1, May 2001 Altera Corporation San Jose, CA (2001).	
	47	"Virtex-II 1.5V Field Programmable Gate Arrays," product specifications DSO3102 (v1.5) April 2, 2001., Xilinx, Inc., San Jose, CA (2001).	
	48	BENDAK et al. "CMOS VLSI Implementation of Gigabyte/second computer network links," proceedings of the IEEE International Symposium on Circuits and Systems '96, pp. 269-272 (1996).	
	49	BONI et al. "LVDS I/O Interface for Gb/s-per-Pin Operation in 0.35-um CMOS," IEEE Journal of Solid-State Circuits, 36:706-711 (2001).	
	50	ESCH et al. "Theory and Design of CMOS HSTL I/O Pads," The Hewlett Packard Journal (1998).	

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